REMARKS

Claims 1-17, 19-42, and 45-47 are pending in the present application. Claims 18, 43, 44, and 48-50 have been cancelled without prejudice or disclaimer to the subject matter contained therein.

A. Rejection of Claims 1, 2, and 7 as being anticipated by Young et al.

Claims 1, 2, and 7 have been rejected under 35 U.S.C. §102(e) as being anticipated by Young et al. (US-A-6,768,338). This rejection under 35 U.S.C. §102(e) is respectfully traversed.

As respectfully demonstrated in the attached Declaration under 37 C.F.R. 1.131, the Applicants reduced to practice the claimed subject, as set forth in claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005, before January 30, 2003, the filing date of US Patent Number 6,768,338.

Moreover, in the alternative, as respectfully demonstrated in the attached Declaration under 37 C.F.R. 1.131, the Applicants conceived the claimed subject, as set forth in claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005, before January 30, 2003, the filing date of US Patent Number 6,768,338 and diligently pursued the preparation of a patent application directed to the claimed subject, as set forth in claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005.

Therefore, in view of the statements made in the attached Declaration under 37 C.F.R. 1.132, Young et al. is not a valid prior art reference under 35 U.S.C. §102(e) because the claimed invention corresponding to claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005 was reduced to practice before January 30, 2003, the filing date of Young et al. (US Patent Number 6,768,338). Moreover, in the alternative, in view of the statements made in the attached Declaration under 37 C.F.R. 1.132, Young et al. is not a valid prior art reference under 35 U.S.C. §102(e) because the claimed invention corresponding to claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005 was conceived before January 30, 2003, the filing date of Young et al. (US Patent Number 6,768,338) and the preparation of a patent application directed was diligently pursued.

Accordingly, in view of the attached Declaration under 37 C.F.R. 1.131 and remarks, the Examiner is respectfully requested to reconsider and withdraw this rejection under 35 U.S.C. §102(e) over Young et al.

B. Rejection of Claims 47-50 as being anticipated by Tanaka et al.

Claims 47-50 have been rejected under 35 U.S.C. §102(b) as being anticipated by Tanaka et al. (US-A-5,514,992). This rejection under 35 U.S.C. §102(b) to claims 47-50 is respectfully traversed.

As respectfully submitted above, amended independent claim 47 sets forth a series connected dual-gate transistor, comprising a first gate and a second gate. The first gate has a gate width and a gate length. The second gate has a gate width and a gate length. The gate length of the first gate is a different size from the gate length of the second gate. The gate width of the first gate is a different size from the gate width of the second gate.

In formulating the rejection under 35 U.S.C. §102(b), the Examiner alleges that Tanaka et al. teaches a switch having a plurality of field effect transistors (**FET2-2, FET2-1, FET3**) connected in series. The Examiner further alleges that Tanaka et al. teaches that each field effect transistor includes a gate, a source, and a drain wherein the gate of one of the series connected field effect transistors is a different size from the gate of another series connected field effect transistor. This position by the Examiner is respectfully traversed.

Tanaka et al. teaches one embodiment wherein the gates' widths are of different sizes, and teaches a separate embodiment wherein the gates' lengths are of different sizes. Tanaka et al. fails to teach a single embodiment wherein both gates' widths are of different sizes and the gates' lengths are of different sizes.

In contrast, amended independent claim 47 states that the gate length of the first gate is a different size from the gate length of the second gate, and the gate width of the first gate is a different size from the gate width of the second gate.

In summary, Tanaka et al. only teaches one embodiment wherein the gates' widths are of different sizes, and teaches a separate embodiment wherein the gates' lengths are of different sizes. Therefore, since Tanaka et al. only teaches one embodiment wherein the gates' widths are of different sizes and a separate embodiment wherein the gates' lengths are of different sizes,

Tanaka et al. fails to anticipate a single embodiment wherein both gates' widths are of different sizes and the gates' lengths are of different sizes, as set forth by the amended independent claim 47.

Accordingly, in view of the amendments and remarks set forth above, the Examiner is respectfully requested to reconsider and withdraw the present rejection.

C. Rejection of Claims 1, 2, and 7 as being unpatentable over Young et al.

Claims 3-6 have been rejected under 35 U.S.C. §103 as being unpatentable over Young et al. (US-A-6,768,338). This rejection under 35 U.S.C. §103 is respectfully traversed.

As respectfully demonstrated in the attached Declaration under 37 C.F.R. 1.131, the Applicants reduced to practice the claimed subject, as set forth in claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005, before January 30, 2003, the filing date of US Patent Number 6,768,338.

Moreover, in the alternative, as respectfully demonstrated in the attached Declaration under 37 C.F.R. 1.131, the Applicants conceived the claimed subject, as set forth in claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005, before January 30, 2003, the filing date of US Patent Number 6,768,338 and diligently pursued the preparation of a patent application directed to the claimed subject, as set forth in claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005.

Therefore, in view of the statements made in the attached Declaration under 37 C.F.R. 1.132, Young et al. is not a valid prior art reference under 35 U.S.C. §103 because the claimed invention corresponding to claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005 was reduced to practice before January 30, 2003, the filing date of Young et al. (US Patent Number 6,768,338). Moreover, in the alternative, in view of the statements made in the attached Declaration under 37 C.F.R. 1.132, Young et al. is not a valid prior art reference under 35 U.S.C. §103 because the claimed invention corresponding to claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005 was conceived before January 30, 2003, the filing date of Young et al. (US Patent Number 6,768,338) and the preparation of a patent application directed was diligently pursued.

Accordingly, in view of the attached Declaration under 37 C.F.R. 1.131 and remarks, the Examiner is respectfully requested to reconsider and withdraw this rejection under 35 U.S.C. §103 over Young et al.

ENTRY OF AMENDMENTS UNDER 37 C.F.R. 1.116

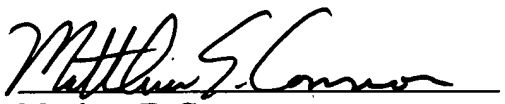
The Applicants respectfully request the Examiner enter the above amendments under 37 C.F.R. 1.116 for the following reasons. As clearly shown above, the attached Declaration places the claims in condition for allowance without raising any new issues of materiality. Moreover, the attached Declaration clearly reduces the outstanding issues in the present application and places the application in better condition for appeal.

Furthermore, as clearly shown above, the amendment to claim 47 places this claim in condition for allowance without raising any new issues of materiality. Moreover, the amendment to claim 47 clearly reduces the outstanding issues in the present application and places the application in better condition for appeal. Thus, entry of the Declaration and the amendments under 37 C.F.R. 1.116 is proper and respectfully requested.

CONCLUSION

Accordingly, in view of the amendments and remarks set forth above, the Examiner is respectfully requested to reconsider and withdraw all the present rejections. Also, an early indication of allowability is earnestly solicited.

Respectfully submitted,



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MEC/MJN/mjn

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Yibing **ZHAO** et al.	**GROUP:**	2819
SERIAL NO:	**10/620,395**	**EXAMINER:**	A. Tran
FILED:	July 16, 2003	**CONFIRMATION:**	9544

FOR: **HIGH POWER, HIGH LINEARITY AND LOW INSERTION LOSS SINGLE POLE DOUBLE THROW TRANSMITTER/RECEIVER SWITCH**

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313–1450

Sir:

DECLARATION UNDER 37 C.F.R. 1.131

WE; Yibing Zhao, Shuyun Zhang, and Robert J. McMorrow; the Applicants of the above-identified application, declare and say, based upon our information and belief:

1. That we conceived the claimed subject, as set forth in claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005, before January 30, 2003, the filing date of US Patent Number 6,768,338;

2. That we reduced to practice the claimed subject, as set forth in claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005, before January 30, 2003, the filing date of US Patent Number 6,768,338;

3. That page A4 of Attachment A provides evidence that we reduced to practice, computer simulation, the claimed subject, as set forth in claims 1, 2, and 7 of the above-

identified application as presented in the Response dated February 14, 2005, before January 30, 2003, the filing date of US Patent Number 6,768,338;

4. That Attachment A provides evidence that we submitted an enabling written description of the claimed subject, as set forth in claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005, before January 30, 2003, the filing date of US Patent Number 6,768,338;

5. That Attachment B provides an enabling written description of the claimed subject, as set forth in claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005, before January 30, 2003, the filing date of US Patent Number 6,768,338;

6. That the written description of Attachment B provides evidence that we conceived the claimed subject, as set forth in claims 1, 2, and 7 of the above-identified application as presented in the Response dated February 14, 2005, before January 30, 2003, the filing date of US Patent Number 6,768,338;

7. That Mr. Matthew E. Connors, the attorney of record, received, on January 16, 2003, a request to accept Attachments A and B and prepare a patent application therefrom; and

8. That from about April 28, 2003 to the filing of the above-identified application, we work diligently with Mr. Connors to prepare a patent application directed to the subject matter described in Attachment B.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are

punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

July 5, 2005
DATE

YIBING ZHAO

July 5th 2005
DATE

SHUYUN ZHANG

July 5th 2005
DATE

ROBERT J. MCMORROW

Attachment A

INVENTION DISCLOSURE

****
****

For Legal Department use only

Disclosure No.: ARD2388HC **Date Submitted:**_

Division: _____ **Vice President:** _____

Cost Center No. 4534

****

(Where Necessary, Use Reverse Side or Separate Sheet to Complete Answers)

1. Title of the Invention:

High Power, High Linearity and Low Insertion Loss SPDT T/R Switch

[Note: The first-listed inventor will be considered the primary inventor and primary contact for patent matters.]

2. Full Name of Inventor No. 1 (including middle name or initial, "Jr.", etc.)

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Vice President: Lew Counts_____ Cost Center #: 4534_____

Product Line: RFPA_____ Supervisor: Rob McMorrow_____

Home Address: 242 Adams Ave._____

Newton, MA 02465_____ Home Telephone: (617) 964-7590_____

Full Name of Inventor No. 2 (including middle name or initial, "Jr.", etc.)

Shuyun Zhang

Analog Address: 804 Woburn St._____ E-Mail Address: shuyun.zhang@analog.com___

Analog Telephone: (781)-937-1240____Division: ALP_____

Vice President: Lew Counts_____ Cost Center #: 4534_____

A1

Product Line: RFPA _____ Supervisor: Rob McMorrow _____

Home Address: _____

_____ _____ Home Telephone: _____

Full Name of Inventor No. 3 (including middle name or initial, "Jr.", etc.)

Rob McMorrow

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Analog Telephone: (781)-937-1966_____ Division: ALP_____

Vice President: Lew Counts_____ Cost Center #: 4354_____

Product Line: RFPA_____ Supervisor: Jay Cormier_____

Home Address: 75 Hayward Mill Rd._____

Concord, MA 01741_____ Home Telephone: 978) 318-0312_____

If more than three inventors, please use separate sheets.

The Invention

3. Brief description of problem solved by invention, and of the invention itself (big-picture overview of invention - may be illustrated by attaching block diagrams, flow charts, etc.):

(See Attached)

4. Detailed description and sketches of invention are to be found on the attached sheets, identified below:

Fig. 1A A schematic diagram of traditional single FET SPDT T/R switch

Fig. 1B A diagram of simplified small signal equivalent circuit model for the SPDT switch structure of Figure 1A

Fig. 1C A drain current vs. gate voltage curve and the swing level of the input RF signal in the FET1 structure of Figure 1A

Fig. 2A A schematic diagram of a traditional three-FET SPDT T/R switch.

Fig. 2B A diagram of simplified small signal equivalent circuit model fo the OFF-state FETs in the three-FET structure of Figure 2A.

Fig. 3 A schematic diagram of the invented three-dual-gate FET SPDT T/R switch in series with modified FET layouts.

Fig. 4A A schematic diagram of the cross-section view of a dual-gate FET_L1 structure of Figure 3.

Fig. 4B A schematic diagram of the cross-section view of a dual-gate FET_L3 structure of Figure 3.

A2

Fig. 4C A schematic diagram of the cross-section view of a dual-gate FET2 structure of Figure 3.

Fig. 5A A diagram of a small signal equivalent circuit for the off-state three dual-gate FET structures of Figure 3.

Fig. 5B A diagram of the simplified small signal equivalent circuit extracted from Figure 5A.

Fig. 6 The curves of simulated Vgs and Vgd as function of time for FET with longer gate length and FET with normal gate size in three dual-gate FETs in series SPDT T/R switch.

Fig. 7 A diagram of the cross-section of a traditional dual-gate HEMT.

5. List any formal drawings, schematics, manuals (by chapter and section), etc. which describe the invention and its operating environment.

Figures #1-7

6. Into what product(s) will this invention go, or what product(s) will this invention be used to make, test, design, etc. (include future generations).

Radio Frequency Power Amplifier Modules (RFPA Modules), high power SPnT switches

Mobile handset terminals for wireless applications.

The Prior Art

7. Closest prior art practices known to the inventor(s), including products/activities of Analog.

Single gate, dual gate, triple gate switches and 2 dual gate SPDT, 3 single gate SPDT and triple gate SPDT switches

8. List any tangible record of prior art/practices known to the inventor(s) e.g., products, patents, manufacturing processes, brochures, printed publications, seminar presentations, product demos, etc.

See above

9. Brief description of the reasons that the invention is different from the prior art practices, and of the advantages resulting from those differences.

Longer gate length and gate width is used to build some of the FETs to improve power handling, linearity. Modifying FET design to decrease resistance in the path channel, i.e. improving insertion loss of switch.

Invention Process and Documentation

10. The invention was first thought of on (date) _____ as evidenced by (notebook entry, etc.) _____

11. The first written description of the invention occurred on (date) _____, a copy of which is attached.

12. The first drawing or sketch occurred on (date) _____, a copy of which is attached.

13. The first disclosure of the invention to others within Analog occurred on (date) __n/a___, as evidenced by _n/a _____

14. The invention was first shown to be operable in its intended environment on (date) _____ by:_ _____

(computer simulation, working prototype, process implementation, etc.) as evidenced by__**design schematic, computer simulation**

[Answer questions 15 and 16 if applicable. If inapplicable, write "N/A" in the appropriate blanks.]

15. The first disclosure of the invention to anyone outside of Analog (if any) occurred on (date)_____ _____ to ___ _____ (pursuant to/not pursuant to a confidentiality [NDA] agreement, dated__ _____, copy attached.)

16. The invention was first sold, sampled, offered for sale, or used to produce a product that ultimately was sold, on (date) _____**n/a**_____ as evidenced by:_____

17. Signature(s) of inventor(s)

(1) _____ Date _____

(2) _____ Date _____

(3)_____ Date _____

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Attachment B

HIGH POWER, HIGH LINEARITY AND LOW INSERTION LOSS SPDT T/R SWITCH

Yibing Zhao, Shuyun Zhang, and Rob McMorrow
Analog Devices, Inc.
804 Woburn Street
Wilmington, MA 01887, USA

Abstract

This invention is used to realize a high performance single-pole-double-throw (SPDT) Transmitter/Receiver (T/R) FET switch. In the design of an electronic switch, low insertion loss, low harmonic distortion and high power handling capability are primarily concerns, and are directly associated with the FET layout and fabrication process. A SPDT switch consists of an antenna port, a transmitter branch coupled to a transmitter port through a plurality of multi-gate FETs in series, and a receiver branch coupled to a receiver port through a plurality of multi-gate FETs in series. When a high power signal passes from the transmitter port to the antenna port through the transmitter branch, the receiver branch is required to be shut off electrically to prevent the high power signal from leaking to receiver port. This leakage will degrade the isolation of the switch and may cause harmonic distortion. Furthermore, the transmitter branch is required to provide a resistance as small as possible to reduce the power loss when it passes through the transmitter branch to the antenna port. Several techniques are known in the industry to improve the isolation and harmonic performance of the switch at the expense of additional circuitry (APD2277-1; US10/235,361). It is an aim of this invention to improve this without adding significant cost or complexity to the design. In our novel receiver branch design, two of the gate metals in the multi-gate FETs are designed with the gate size several times larger than the others. This is used to improve the harmonic distortion and power handling capability. In addition, multi-gate FETs connected to each other in series are applied to improve the insertion loss. The utilization of a heavily-doped cap layer between the gate fingers in a multi-gate FET, furthermore, is benefit to reduce the channel resistance of FET, thereby, lowering the insertion loss.

Technical Field

The present invention relates to high frequency semiconductor switches used for wireless communication systems, particularly to high-electron-mobility-transistor (HEMT) switches to meet the criteria of high power, low insertion loss, and low distortion performance.

Background of the Invention

In mobile wireless communication systems, especially GSM cellular handsets, the transmit/receive (T/R) switch applied to the antenna end is capable of handling a high power signal of up to 35 dBm along with low harmonic distortion and low signal loss.

The control voltage for switching is limited by the handset battery voltage of 3 Volts and, in some cases, even less.

Figure 1A is a schematic diagram of a traditional SPDT FET switch. When the control voltage V_{cont1} is 0V and V_{cont2} is 3V, FET1 is in OFF state because the voltage drop between the gate and source, $V_{g1s1} = V_{g1}-V_{s1}$, or gate and drain, $V_{g1d1} = V_{g1} - V_{d1}$, in FET1 is below FET pinch-off voltage, V_p; while FET2 is in ON state because $V_{g2s2} = V_{g2}-V_{s2}$ or $V_{g2d2} = V_{g2} - V_{d2}$ is beyond V_p in FET2. When a high power RF signal passes through the on-state FET2 to antenna, it is applied to the off-state FET1 at the antenna port as well. Due to extremely low resistance loss in FET2, FET2 remains in the ON State no matter how high a power is applied. Essentially, the power loss and generation of distortion are related to the change in operational status of FET1. This can be verified through the simulation of the simplified small-signal equivalent circuit model of FET1, as shown in Figure 1B. Assuming that the RF signal is $v+ = V|_{rf} \cdot Sin(\omega t)$, voltage drop in each junction of FET1 is expressed as below:

$$V_{g1s1} = V_{gs}(DC) + \frac{C_{gd1}}{C_{gd1} + C_{gs1}} \bullet \tilde{V} \qquad (1)$$

$$V_{g2d2} = V_{gd}(DC) - \frac{C_{gs1}}{C_{gd1} + C_{gs1}} \bullet \tilde{V} \qquad (2)$$

where $V_{gs}(DC)$ and $V_{gd}(DC)$ are DC voltage drops in each junction in FET1, respectively. Normally, $V_{gd}(DC) = V_{gs}(DC) \geq V_{cont1} - V_{cont2} = -3V$; $C_{gs1} = C_{gd1}$ in a symmetric designed FET1; $V|_{rf} = 17.8$ V for 35 dBm RF signal, and $V_p = -1V$ which is the most popular pinch-off value in a HEMT design, then

$$V_{g1s1} = -3 + 8.9 \bullet Sin(\omega t) \qquad (3)$$

$$V_{g1d1} = -3 - 8.9 \bullet Sin(\omega t) \qquad (4)$$

From Expression (3) and (4), it can be seen that V_{g1s1} is higher than V_p in a certain time period when v+ is in the positive half cycle, and V_{g1d1} is higher than V_p in a certain time period when v+ is in the negative half cycle. Therefore, FET1 is not able to remain in the OFF state at all times, causing power loss and harmonic distortion. The capability of power handling in a single FET switch can be estimated based on the drain current vs. gate-source voltage curve in Figure 1C. The maximum power transfer without distortion is achieved by keeping FET1 in OFF state. Hence,

$$\bar{V}_{rf\,max} = \left| V_{cont1} - V_{cont2} - V_p \right| \bullet \frac{C_{gs1} + C_{gd1}}{C_{gd1}} \qquad (5)$$

So, the maximum power, $P_{rf\,max}$, is obtained in Expression (6),

$$P_{rf\max} = \frac{1}{2Z_0}\left(\frac{C_{gs1} + C_{gd1}}{C_{gd1}}\right)^2 \left(V_{cont1} - V_{cont2} - V_p\right)^2 \qquad (6)$$

where Z_0 is the system impedance, normally equal to 50 Ω. In a symmetric FET switch, $P_{rf\max}$ is calculated to be 22 dBm which is much less than the specification for SPDT switches used in cellular handset applications.

It is seen from Expression (6) that lowering pinch-off voltage and increasing control voltage effectively improves power handling capability and suppress harmonic distortion. However, the battery, as mentioned above, limits the control voltage, and the on-state FET resistance R_{on} restricts V_p. In other words, the lower the V_p, the higher insertion loss. Therefore, both methods do not have enough margin to be changed. Another approach to increase power handling capability is to use a plurality of FETs in series to replace single FET SPDT switches as shown in Figure 2A, a traditional three-FET SPDT switch. Similarly, maximum transmit power with extremely low harmonic distortion can be derived based on the small signal equivalent circuit in Figure 2B,

$$P_{rf\max} = \frac{9}{2Z_0}\left(\frac{C_{gs} + C_{gd}}{C_{gd}}\right)^2 \left(V_{cont1} - V_{cont2} - V_p\right)^2 \qquad (7)$$

where, assuming all three FETs are identical, i.e. $C_{gs1} = C_{gs2} = C_{gs3} = C_{gs}$, $C_{gd1} = C_{gd2} = C_{gd3} = C_{gd}$. Taking the parameters for a single FET, the maximum power $P_{rf\max}$ without distortion in three-FET switch can be calculated as 31.5 dBm according to Expression (7). Compared to 22 dBm of $P_{rf\max}$ in a single FET switch, it clearly indicates that more FETs in series can improve power handling capability of the switch. $P_{rf\max}$ for n FETs in series can be easily deduced from Expression (7) as follows,

$$P_{rf\max} = \frac{n^2}{2Z_0}\left(\frac{C_{gs} + C_{gd}}{C_{gd}}\right)^2 \left(V_{cont1} - V_{cont2} - V_p\right)^2 \qquad (8)$$

The correlation of switch insertion loss in the transmitter branch and FET characteristics is written below,

$$IL \approx -20\log\left(1 + \frac{R_{on}}{2Z_0}\right) \qquad (9)$$

$$R_{on} \propto \frac{nL_g}{W_g\left(V_{cont1} - V_{cont2} - V_p\right)} \qquad (10)$$

where IL is the insertion loss in dB, R_{on} is the total resistance of on-state FETs in the transmitter branch, W_g is the gate width of each FET, and L_g is the gate length of each FET. Expression (8) to (10) indicate that in a traditional SPDT switch, an increase of the number of FETs in series enhances the power handling capability and reduces signal distortion. On the other hand, the more FETs in series leads to higher insertion loss. In addition, the increase of insertion loss caused by the reduction of V_p as mentioned above,

is confirmed through the correlation of R_{on} and V_p in Expression (10). An optimum arrangement has been proposed in US10/235,361 (APD2277-1), where three dual-gate FETs have been used in series for a total of 6 gates.

To solve these fundamental problems in SPDT T/R switches, a novel plurality of dual-gate FETs in series with a modified gate formation has been designed to provide high power handling capability, low harmonic distortion, and low insertion loss.

Summary of the Invention

In the invention, a SPDT T/R switch composed of a plurality of dual-gate metal-semiconductor field-effect transistors (MESFETs) or dual-gate HEMTs are connected in series and coupled to a receiver port and an antenna port, and a plurality of dual-gate MESFETs or HEMTs are connected in series and coupled to a transmitter port and an antenna port. Two gate metals in two of the FETs, respectively, are fabricated with a gate size several times larger than the others. One of the large sized gates is positioned closer to source (or drain) port than to drain (or source). The second large sized gate is positioned in the opposite way, closer to drain (or source) than to source (or drain) port. The longer gate size is realized by making the gate length N times longer than the others and by increasing the gate width. The increased gate size results in larger parasitic capacitances between the gate to its surrounding metals, such as source port and drain port. The reduced space between the gate to neighbor metals leads to further increases in the parasitic capacitance while the series resistance is reduced. Therefore, the distribution of RF signal on each off-state FET in the receiver branch is modified, and is different from the traditional switch where the RF signal is uniformly distributed across all off-state FETs. The voltage swing in the junction of the large gate size FET is significantly reduced so that the OFF state is maintained. Thus, the modifications in the FET design enhance the power handling capability and reduce the creation of harmonic distortion. A similar effect is achieved in US10/235,361 (APD2277-1) by using external capacitors connected between the gate and source (or drain). Creating this device parasitic eliminates the need for these external capacitors.

The on-state resistance R_{on} can be reduced by the decrease in space of gate to drain port or gate to source as mentioned above. In the invention, R_{on} in dual-gate FETs, even triple-gate FETs, furthermore, is reduced by designing a heavily-doped semiconductor cap layer on top of the area between gate metals, thereby, improving the insertion loss in the T/R switch.

According to the content in the invention, a dual-gate FET SPDT switch with modified gate sizes exhibits low distortion and high power handling capability without the need for additional circuitry. The modifications of the HEMT layout design results in the reduction of HEMT SPDT switch insertion loss. Additionally, by eliminating the need for external capacitors, this novel design can greatly improve the resilience to electrostatic discharge (ESD), which can cause catastrophic damage.

Brief Description of the Drawings

Figure 1A is a schematic diagram of traditional single FET SPDT T/R switch.

Figure 1B is a diagram of simplified small signal equivalent circuit model for the SPDT switch structure of Figure 1A.

Figure 1C is a drain current vs. gate voltage curve and the swing level of the input RF signal in the FET1 structure of Figure 1A.

Figure 2A is a schematic diagram of a traditional three-FET SPDT T/R switch.

Figure 2B is a diagram of simplified small signal equivalent circuit model for the OFF-state FETs in the three-FET structure of Figure 2A.

Figure 3 is a schematic diagram of the invented three dual-gate FETs SPDT T/R switch in series with modified FET layouts.

Figure 4A is a schematic diagram of the cross-section view of a dual-gate FET_L1 structure of Figure 3.

Figure 4B is a schematic diagram of the cross-section view of a dual-gate FET_L3 structure of Figure 3.

Figure 4C is a schematic diagram of the cross-section view of a normal dual-gate FET2 structure of Figure 3.

Figure 5A is a diagram of a small signal equivalent circuit for the off-state three dual-gate FET structures of Figure 3.

Figure 5B is a diagram of the simplified small signal equivalent circuit extracted from Figure 5A.

Figure 6 is a diagram of simulated V_{gs} and V_{gd} as function of time for FET with longer gate length and FET with normal gate size in three dual-gate FETs in series SPDT T/R switch.

Figure 7 is a diagram of cross-section of a traditional dual-gate HEMT.

Detailed Description of the Invention

A dual-gate FET T/R switch with modified gate sizes is invented to improve the switch linearity under a high power signal. As shown in Figure 3, three dual-gate FETs are connected in series between the antenna port and receiver port and between the antenna port and transmitter port. The cross-sections of transistors FET_L1, FET2 and FET_L3 are shown in Figure 4A, 4B and 4C, respectively. In all drawings, the key

equivalent circuit parameters are described physically. To explain the advantages of this invented switch, a small signal equivalent circuit model of the receiver branch (Off-state FETs) is plotted in Figure 5A. Because of extremely large channel resistance R_{ch} in each transistor in OFF state, the small signal model in Figure 5A can be simplified as shown in Figure 5B. The control voltage is applied to each gate through an extremely large resistor R that prevents the RF signal from bleeding to the DC control voltage source. The voltage at gate port is expected to be the same as V_{cont} at the resistor end. Similar to the analysis of a single FET switch, the voltage drop in each FET junction can be expressed as a function of capacitance and control voltage. Since all FETs with smaller gate sizes are designed symmetrically and have the same gate length, it is assumed that $C_{gisi} = C_{gidi}$ (i = 2 to 5), where $C_{gisi} = C_{gsi} + C_{spi}$ and $C_{gidi} = C_{gdi} + C_{dpi}$. C_{dpi} and C_{spi} are fringing parasite capacitances which are the function of distance between gate metal to drain and source metals, respectively, as demonstrated in Figure 4A. For gate 1 in FET_L1 and gate 6 in FET_3, $C_{g1s1} = C_{g6d6}$ and $C_{g1d1} = C_{g6s6}$ due to the mirror-like layout. For simplification, let $C_{gisi} = C_{gidi} = C_{off}$ (i=3, 4); $C_{gisi} = C_{gidi} = C'_{off}$ (i = 2, 5); $C_{g1s1} = C_{g6d6} = C_{off1}$, and $C_{g1d1} = C_{g6s6} = C_{off2}$. Then, the voltage drops for long gate G1 in FET_L1 is written as follows,

$$V_{g1s1} = V_{cont1} - V_{cont2} + \frac{1}{\frac{4C_{off1}}{C_{off}} + \frac{4C_{off1}}{C'_{off}} + 2\frac{C_{off1}}{C_{off2}} + 2}\tilde{v} \tag{11}$$

$$V_{g1d1} = V_{cont1} - V_{cont2} - \frac{1}{\frac{4C_{off2}}{C_{off}} + \frac{4C_{off2}}{C'_{off}} + 2\frac{C_{off2}}{C_{off1}} + 2}\tilde{v} \tag{12}$$

The voltage drops for short gate G2 in FET_L1 are written below,

$$V_{g2s2} = V_{cont1} - V_{cont2} + \frac{1}{\frac{4C'_{off}}{C_{off}} + 2\frac{C'_{off}}{C_{off1}} + 2\frac{C'_{off}}{C_{off2}} + 4}\tilde{v} \tag{13}$$

$$V_{g2d2} = V_{cont1} - V_{cont2} - \frac{1}{\frac{4C'_{off}}{C_{off}} + 2\frac{C'_{off}}{C_{off1}} + 2\frac{C'_{off}}{C_{off2}} + 4}\tilde{v} \tag{14}$$

The voltage drops for gate 3 and gate 4 in FET2 can be easily derived similar to Expression (13) and (14). Because of the same FET layout, V_{g3s3} is equal to V_{g4s4}, and V_{g3d3} is equal to V_{g4d4}.

$$V_{g3s3} = V_{cont1} - V_{cont2} + \frac{1}{\frac{4C_{off}}{C'_{off}} + 2\frac{C_{off}}{C_{off1}} + 2\frac{C_{off}}{C_{off2}} + 4}\tilde{v} \quad (15)$$

$$V_{g3d3} = V_{cont1} - V_{cont2} - \frac{1}{\frac{4C_{off}}{C'_{off}} + 2\frac{C_{off}}{C_{off1}} + 2\frac{C_{off}}{C_{off2}} + 4}\tilde{v} \quad (16)$$

In FET_L3, the layout of gate 5, G5 is the same as gate 2, G2 in FET_L1. Thus, $V_{g5s5} = V_{g2s2}$ in Expression (13) and $V_{g5d5} = V_{g2d2}$ in Expression (14). Since the mirror-like layout of gate 6, G6 to gate 1, G1, the expressions of V_{g6s6} and V_{g6d6} are written as follows,

$$V_{g6s6} = V_{cont1} - V_{cont2} + \frac{1}{\frac{4C_{off2}}{C_{off}} + \frac{4C_{off2}}{C'_{off}} + 2\frac{C_{off2}}{C_{off1}} + 2}\tilde{v} \quad (17)$$

$$V_{g6d6} = V_{cont1} - V_{cont2} - \frac{1}{\frac{4C_{off1}}{C_{off}} + \frac{4C_{off1}}{C'_{off}} + 2\frac{C_{off1}}{C_{off2}} + 2}\tilde{v} \quad (18)$$

The operational status of each FET depends on the gate-source voltage V_{gs} (or gate-drain voltage V_{gd}) and pinch-off voltage V_p. As long as either V_{gs} or V_{gd} is less then V_p, i.e. V_{gs}(or V_{gd}) < V_p, the FET is in the OFF state. As mentioned above, to suppress harmonic distortion and enhance power handling in a T/R switch, the leakage of the RF signal from receiver branch to ground must be minimized while the high power RF signal is transmitted to the antenna. This implies that at least one of the FETs in the receiver branch must remain in the OFF state. Before explaining the mechanism of the switch in the invention, the correlation between the parasitic capacitances C_{off}, C'_{off}, C_{off1} and C_{off2} are introduced based on the transistor physical model in Figure 4A, Figure 4B, and Figure 4C. When epitaxy of the FET structure is fixed, the parasitic parameters in the FET equivalent circuit model are directly related to the FET geometric sizes, such as gate length L_g, gate width W_g, space between gate and source port L_{gs}, and space between gate and drain port L_{gd}, etc. Normally, the intrinsic capacitance C_{gs} and C_{gd} are dependent on the gate size, for example,

$$C_{gs} = W_g L_g C_{ox} F_1(V_{ds}) \quad (19)$$

$$C_{gd} = W_g L_g C_{ox} F_2(V_{ds}) \quad (20)$$

where C_{ox} is the capacitance associated with the FET epitaxial structure, and $F_1(V_{ds})$ and $F_2(V_{ds})$ are special functions varying with drain-source voltage. When the FET is OFF, both F_1 and F_2 are constant.

It is demonstrated in the expressions that the longer the gate length, the larger C_{gs} and C_{gd}. Assuming that gate length is N times a standard gate length (normally 0.5 micron), C_{gs} and C_{gd} are increased about the same amount, theoretically. In reality, when a FET operates in a deep OFF state, these intrinsic capacitances are not only proportional to the gate length, but also, to some degree, reversely proportional to the distance between gate metal to the drain or source port, L_{gs} and L_{gd}, respectively. Consequently, C_{gs} and C_{gd} decrease with an increase in L_{gs} and L_{gd}. The reason is because high the resistivity depletion area extends beyond the gate area toward the drain and source electrodes with more negative FET junction biases. This emulates an increase in the distance between two metal plates in a parallel-plate capacitor, leading to the decrease in capacitance. In Figure 4A, it is seen that there are some extrinsic capacitances C_{sp} and C_{dp} generated between electrodes, in addition to the intrinsic capacitances. This kind of capacitor is called a fringing capacitor and behaves like a parallel-plate capacitor. In other words, this capacitance is inversely proportional to the distance between the gate and drain or source port. As with the intrinsic capacitors, the fringing capacitance also increases with the gate width. For the insertion loss of the switch, the large L_{g1} results in a larger channel resistance R_{ch1} in the on-state FET_L1, as indicated in Expression (10). To compensate for this drawback, a longer gate width is designed since R_{on} is inversely proportional to the gate width. Of course, increasing gate width leads to an increase in intrinsic capacitance C_{gs} and C_{gd}, and fringing capacitance C_{sp} and C_{dp}.

Looking into the equivalent circuit model in Figure 4A and Figure 4B, $C_{off1} = C_{g1s1} = C_{gs1} + C_{sp1}$; $C_{off2} = C_{g1d1} = C_{gd1} + C_{dp1}$; $C'_{off} = C_{g2s2} = C_{gs2} + C_{sp2}$. In Figure 4C, C_{off} can be calculated as $C_{off} = C_{g3s3} = C_{gs3} + C_{sp3}$. In a symmetrically designed FET, it is reasonable to let $C_{sp} = C_{dp}$. Assuming that L_{g1} and L_{g6} is N times of L_{g2} (or L_{g3}...), W_g of FET_L1 and FET_L3 is N' times longer than W_g of FET2, then, the correlations among C_{off1}, C_{off2}, C'_{off}, and C_{off} are approximately expressed,

$$\frac{C_{off1}}{C'_{off}} = \frac{NN'C_{gs2} + C_{sp1}}{C_{gs2} + C_{sp2}}, \quad \frac{C_{off1}}{C_{off}} = \frac{NN'C_{gs3} + C_{sp1}}{C_{gs3} + C_{sp3}}, \quad \frac{C_{off1}}{C_{off2}} = \frac{C_{gs1} + C_{sp1}}{C_{gd1} + C_{dp1}} \qquad (21)$$

Because $L_{gs1} < L_{gs2} = L_{gs3} < L_{gd1}$, $C_{sp1} > C_{sp2} = N'C_{sp3}$ and $C_{sp2} > C_{dp1}$. Consequently, $C_{off1}/C_{off} > C_{off1}/C'_{off} > N*N'$, and $C_{off1}/C_{off2} > 1$.

It is worth noticing that the increase in gate width impacts another parasitic capacitor, C_{ds}. C_{ds} in the OFF-state FET plays a role in the isolation performance which is another figure of merit for a SPDT switch. This determines the RF energy leaks from the antenna port to the OFF port, or vice versa. Normally, increasing C_{ds} deteriorates isolation of the off-state FET. In this invention, however, the longer gate length compensates the increase in Cds because the physical distance between drain and source

is extended. Therefore, the resulting C_{ds} basically remains the same as that of FET with normal gate length and gate width.

In Expression (11) and (18), the third item is much less than v+ /(8N*N' + 4), while the third items in the other FET junctions, such as V_{g3s3} (Expression 15) and V_{g3d3} (Expression 16) is about v+ /(8 + 4/N*N'). In the case of three dual-gate FETs in series without modification of gate size, the third item is 1/12v+. This implies that the fluctuation of voltage drop of the junction G1S1 and G6D6 due to the transmitted RF signal is dramatically reduced compared with those of other junctions in the invented switch. As long as this fluctuation is less than $|V_{cont1}-V_{cont2}-V_p|$, this FET remains off. For example, let N = N' = 2, and assuming $V_{cont1}-V_{cont2}$ = -2.6 V (self-biasing due to the gate current causes the DC voltage drop to be less than the difference in control voltages, –3 V), the junction voltages can be simulated according Expressions (11) to (18). In this simulation, $P_{rf\,max}$ = 37 dBm, V_p = -1V, $\omega = 2\pi f_0$ = 1 GHz. Figure 6 is the simulation results of some voltage swings in the FET junctions vs. time. It is clear that in the first half period of the RF signal v+, V_{g1s1} changes from deep negative to shallow negative, but remains below V_p, while V_{g1d1} becomes more negative. Thus, FET_L1 remains in the OFF state while FET_L3 and FET2 turn on for some time period due to the junction voltage exceeding V_p. Similarly, in the second half period of the RF signal v+, V_{g6d6} and V_{g6s6} remain below V_p so that FET_L3 stays in the OFF state while FET2 and FET_L1 turn on. The results indicate that at least one of the FETs in the receiver branch remains in the OFF state for the full RF cycle, thus, preventing power leakage from the receiver branch and significantly improving the harmonic distortion. The power handling capability is enhanced as well due to the better isolation.

As mentioned in the summary of invention section, in HEMT switches, the on-state resistance between two gate metals can be reduced in this invention by designing a n+ cap layer on top of the transistor connection area, as shown in Figure 4A, 4B, and 4C. Looking into a traditional dual-gate HEMT design in Figure 7, the heavily-doped cap layer between gate fingers is chemically etched off. Consequently, the surface potential, $V_{surface}$, can easily deplete the non-doped exposed layer, resulting in a decrease in the electrical carrier density, and consequent increase in resistance R_{gg} in this segment. Normally, the total resistance in an on-state dual-gate FET can be written as,

$$R_{tot} = 2R_s + 2R_{ch} + R_{gg} \qquad (22)$$

High R_{gg} causes high R_{tot}, thereby, leading to high R_{on}. In a traditional HEMT structure, R_s is about 0.12 Ω-mm, R_{ch} is about 1.2 Ω-mm for a 0.5 μm gate length in ON state transistor, and R_{gg} is about 0.7 Ω-mm without cap layer. The theoretical effect of R_{gg} on the insertion loss in an SPDT switch can be calculated as follows. Assuming a gate width of 1 mm, three dual-gate HEMTs in series create an ON state resistance R_{on} of about 6.1 Ω. According to Expression (9), the insertion loss is about 0.52 dB. With the modified layout, the heavily-doped cap layer screens any surface potential change, which helps to minimize the channel resistance in this segment. In this case, R_{gg} is about 0.25 Ω-mm. Thus, R_{on} is estimated as 4.7 Ω, i.e., 0.4 dB insertion loss. It indicates that the

application of the cap layer on top of the connection area dramatically improves the insertion loss.

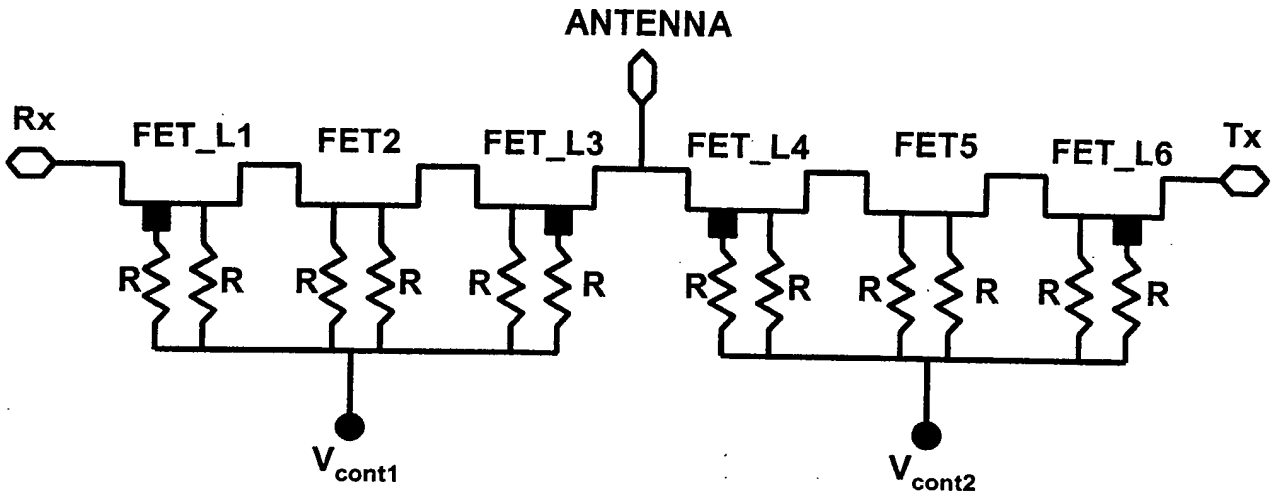


Figure for this invention

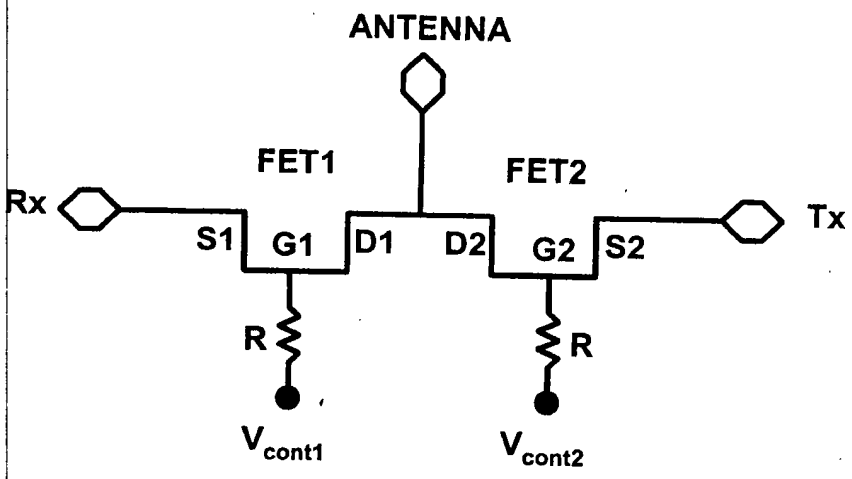


Figure 1A

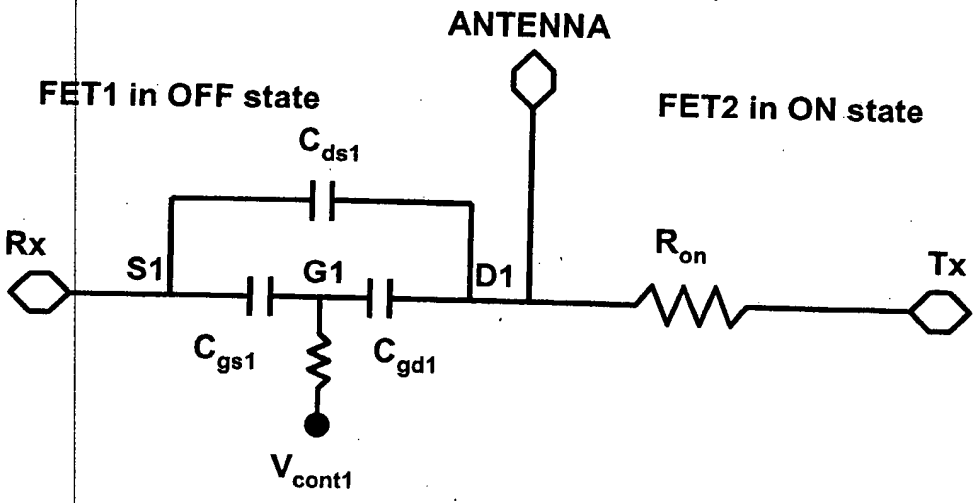


Figure 1B

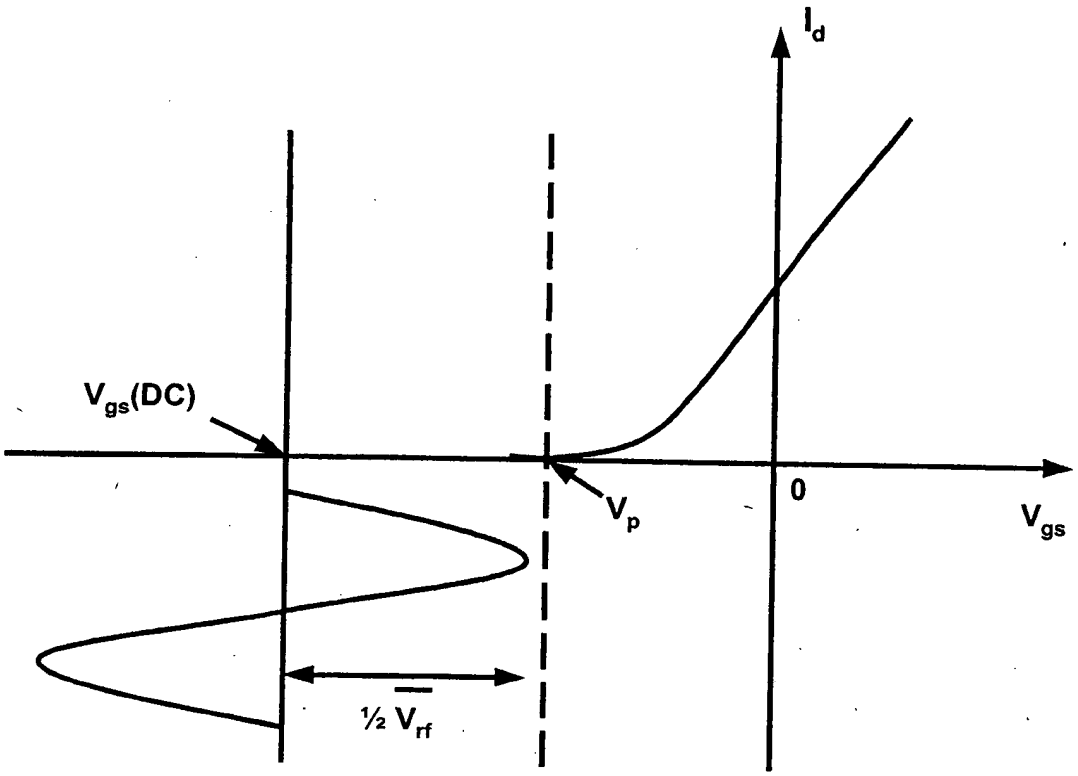


Figure 1C

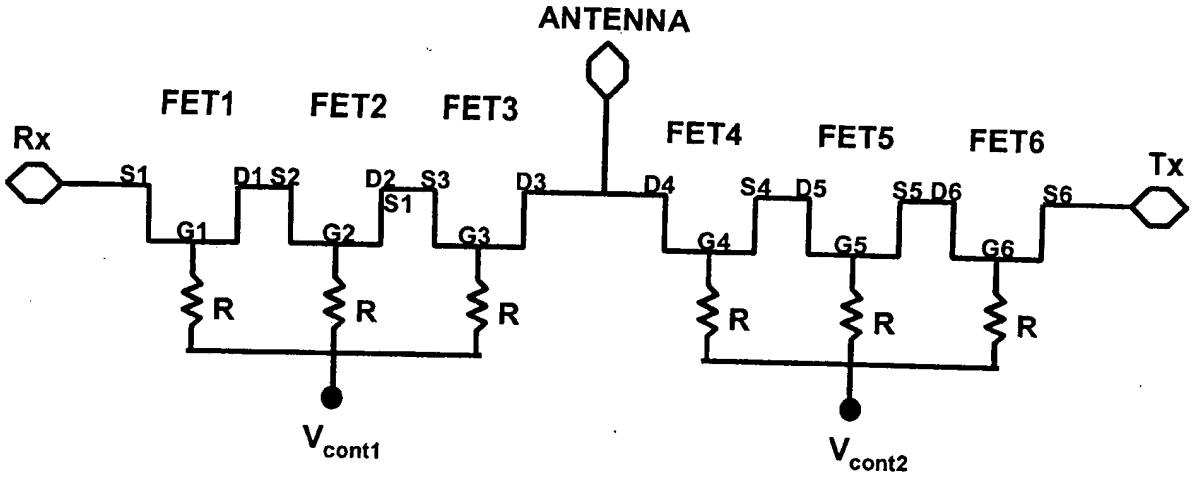


Figure 2A

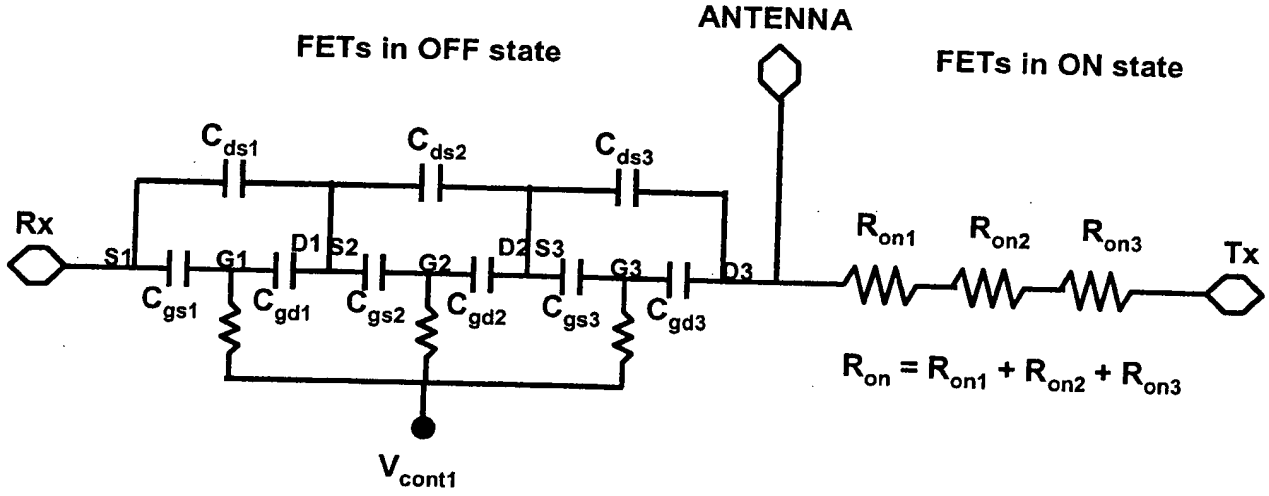
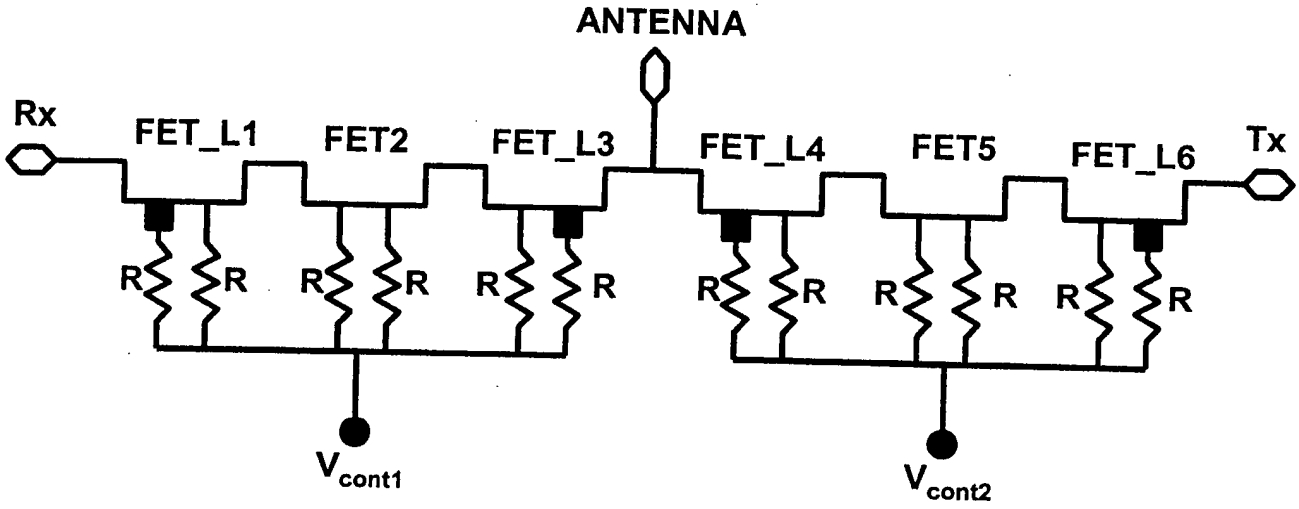


Figure 2B



■ This symbol represents the larger gate length

Figure 3

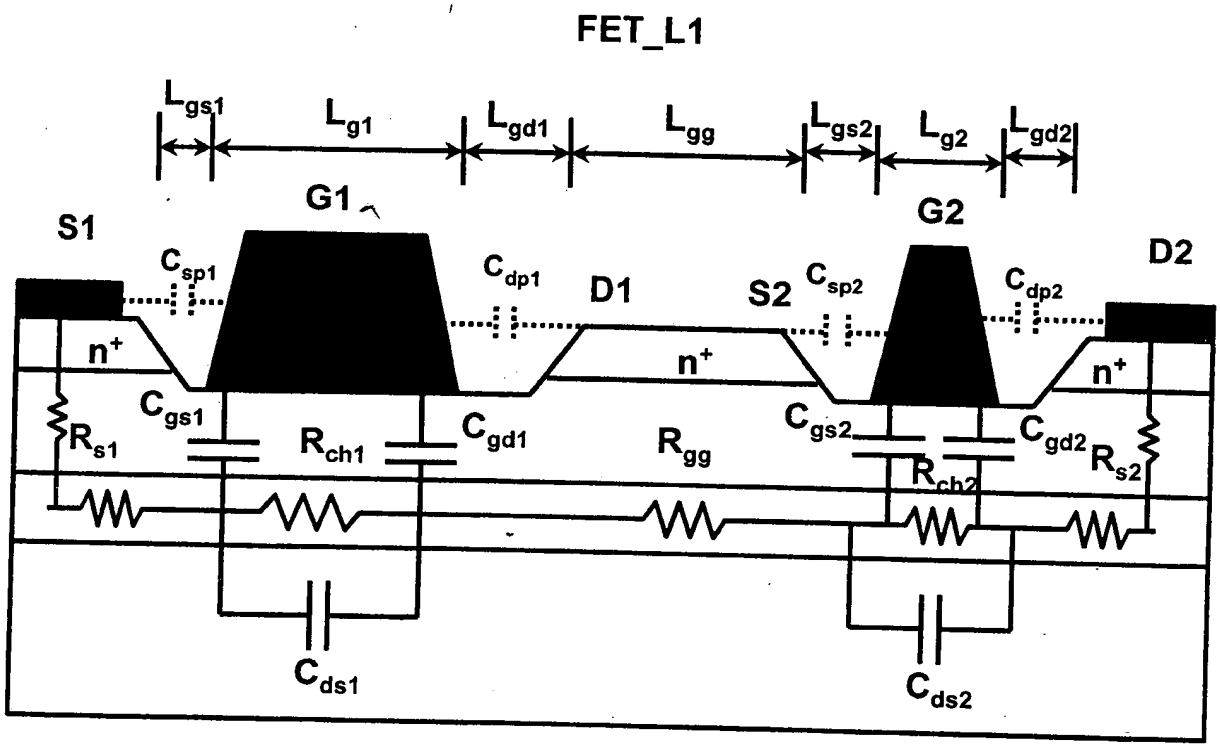

FET_L1
L_{gs1}
L_{g1}
L_{gd1}
L_{gg}
L_{gs2}
L_{g2}
L_{gd2}
S1
G1
G2
D2
D1
S2
C_{sp1}
C_{dp1}
C_{sp2}
C_{dp2}
n^+
n^+
n^+
C_{gs1}
R_{s1}
R_{ch1}
C_{gd1}
R_{gg}
C_{gs2}
C_{gd2}
R_{ch2}
R_{s2}
C_{ds1}
C_{ds2}

Figure 4A

FET_L3

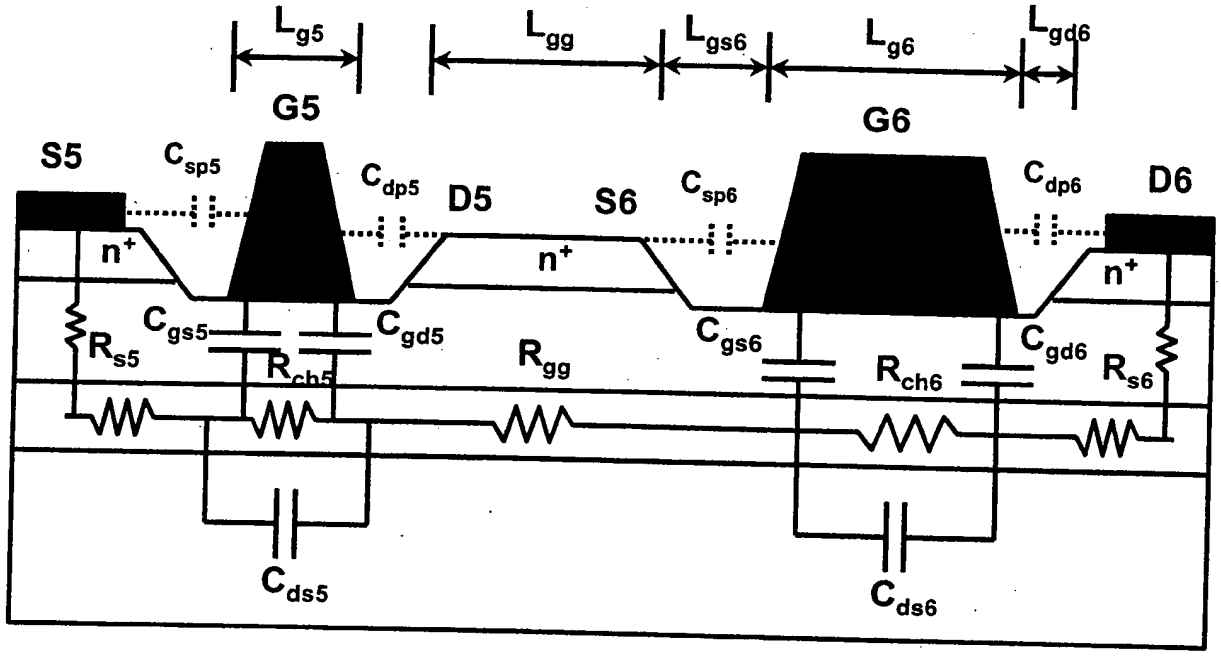


Figure 4B

FET_2

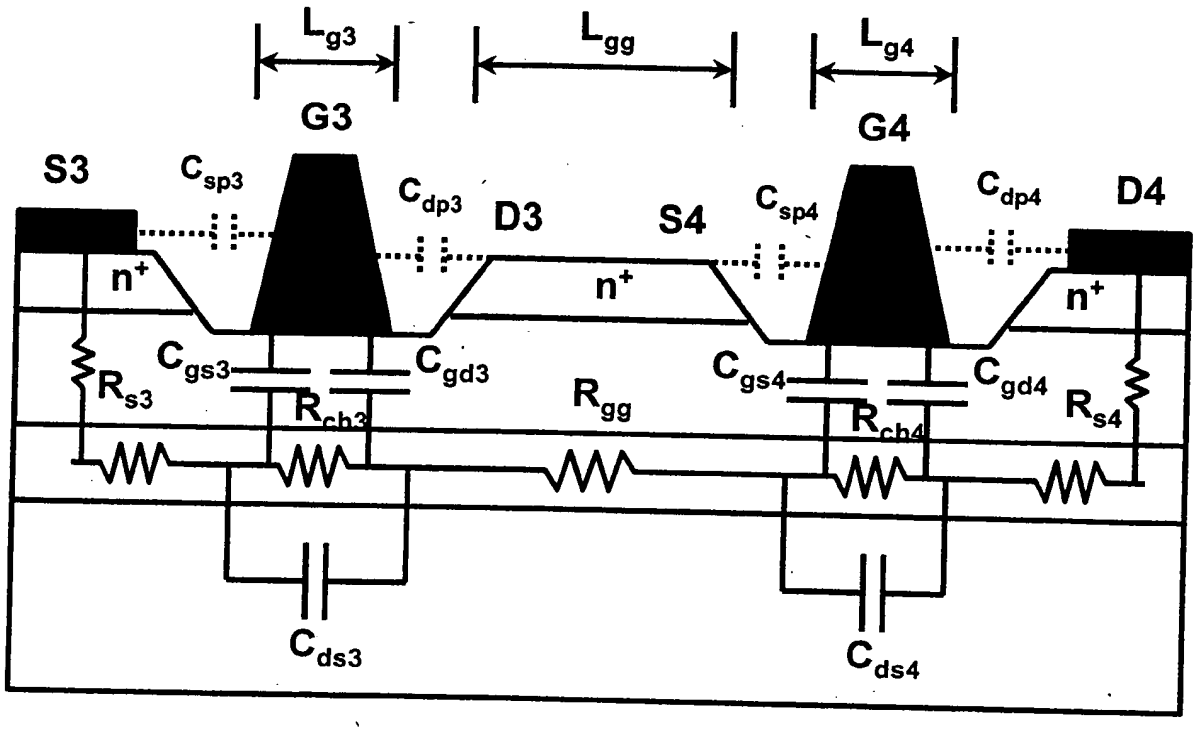


Figure 4C

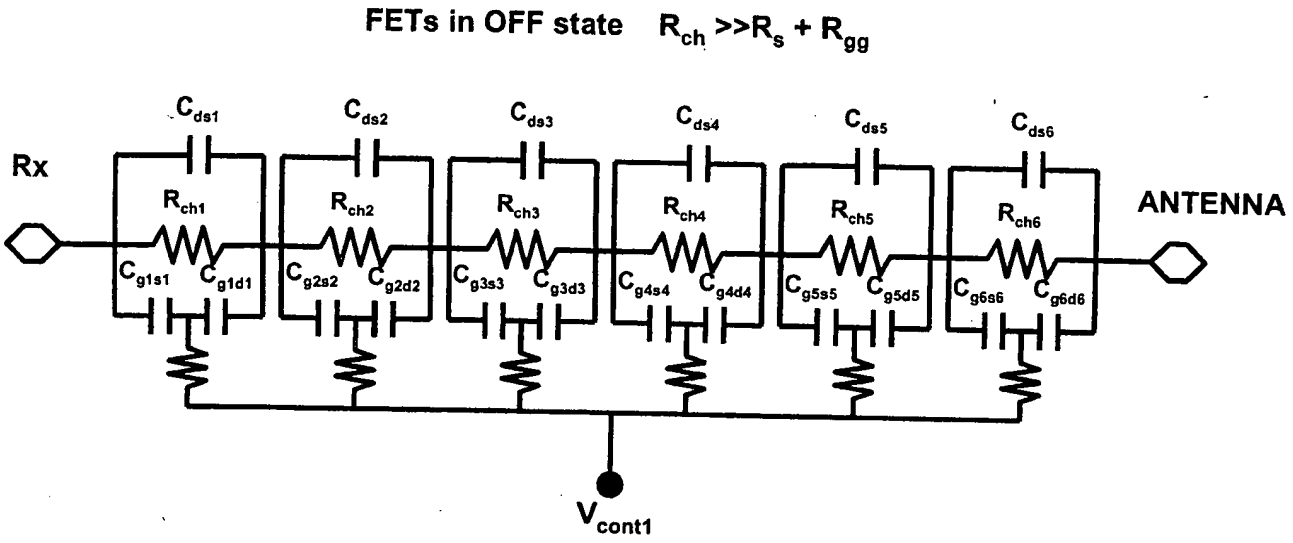


Figure 5A

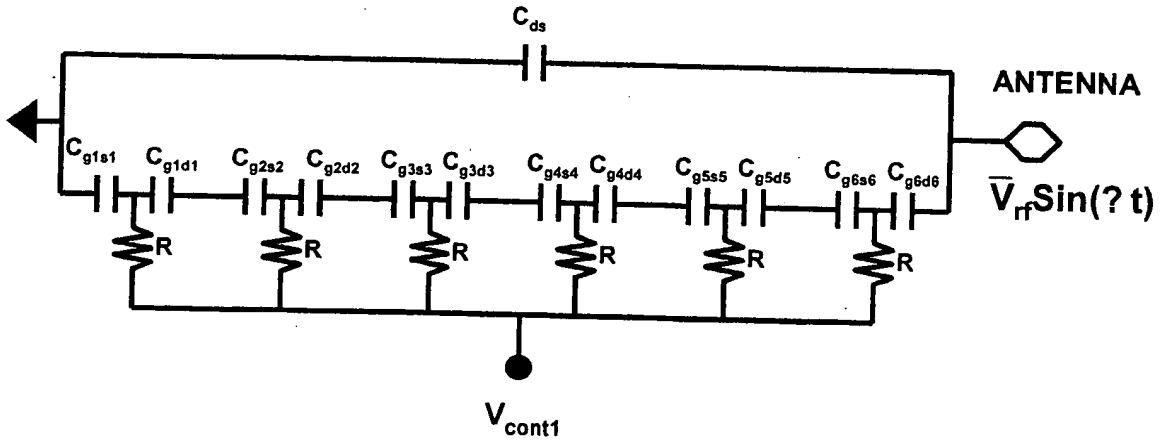


Figure 5B

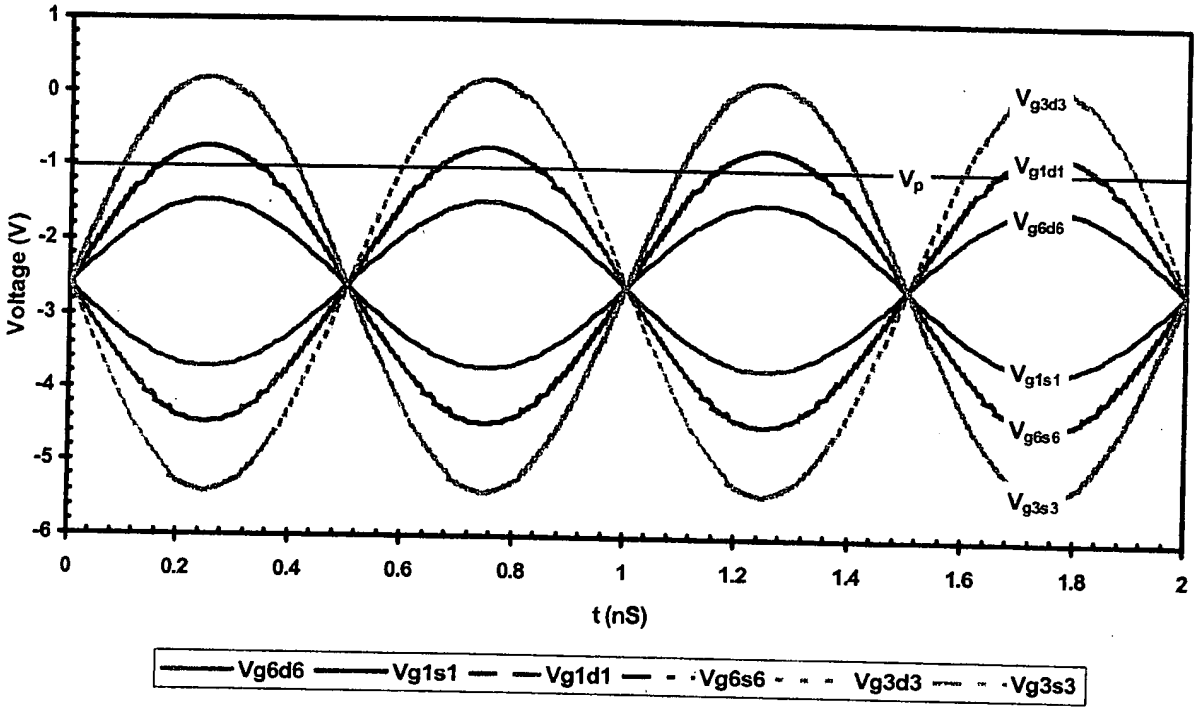

1
0
-1
-2
-3
-4
-5
-6
Voltage (V)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
t (nS)
V_{g3d3}
V_{g1d1}
V_p
V_{g6d6}
V_{g1s1}
V_{g6s6}
V_{g3s3}
Vg6d6
Vg1s1
Vg1d1
Vg6s6
Vg3d3
Vg3s3

Figure 6

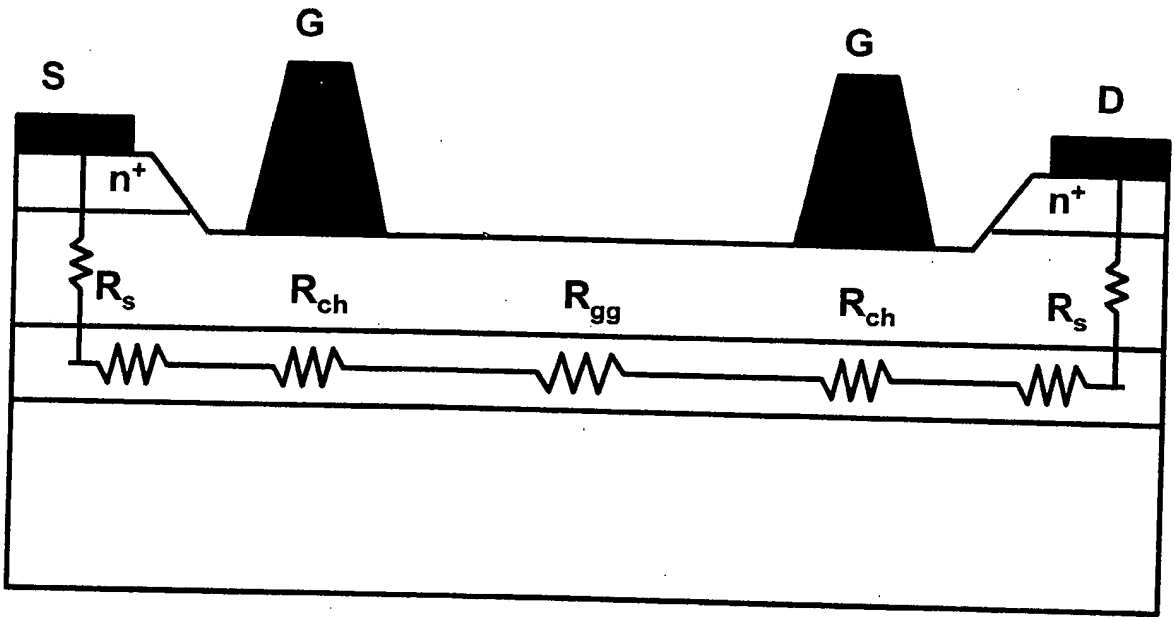


Figure 7